

In the Claims:

1. (Currently Amended) A method of ~~cleaning-removing surface oxide from the surface of a~~  
~~conductive layer forming the bottom of a hole~~ formed in an organic inter-level dielectric (ILD),  
the hole having sidewalls and ~~[[a ]]said~~ bottom, the organic ILD disposed on a semiconductor  
substrate, the method comprising:

performing a radio frequency (RF) sputter clean of the hole ~~to remove said surface oxide;~~

and

performing an anisotropic, ion enhanced etch, ~~at least partially during the sputter clean,~~ of  
organic material ~~displaced from the sidewalls of the hole and deposited [[in ]]at the bottom of the~~  
~~hole by the sputter clean. hole at least partially during the sputter clean,~~

~~whereby organic material displaced from the sidewalls to the bottom of the hole by the~~  
~~sputter clean is removed by the anisotropic organic etch.~~

2. (Previously Presented) The method of claim 1, wherein the ion enhanced etch of the  
organic material comprises a nitrogen plasma.

3. (Previously Presented) The method of claim 24, wherein the RF sputter clean comprises  
an argon plasma.

4. (Previously Presented) The method of claim 24, wherein the RF sputter clean comprises  
a helium plasma.

5. (Canceled)

6. (Currently Amended) The method of claim 24, wherein the anisotropic ion enhanced etch of the organic ~~material~~ particles comprises a nitrogen plasma.
7. (Currently Amended) The method of claim 24, wherein the anisotropic, ion enhanced etch of the organic ~~material~~ particles is ion enhanced with an RF bias of between about 0 watts and about 500 watts.
8. (Currently Amended) The method of claim 24, wherein the RF sputter clean and the ~~organic~~ anisotropic, ion enhanced etch are performed over about the same time interval.
9. (Canceled)
10. (Currently Amended) A method of ~~cleaning an~~ removing surface oxide from the surface of a conductive interconnect structure formed in an organic ILD, the structure comprising a hole having a bottom formed by the surface of said conductive interconnect structure and sidewalls, the structure disposed on a semiconductor substrate, the method comprising:
  - forming a plasma over the interconnect structure, the plasma comprising a physical etch component and an ion enhanced chemical etch component;
  - directing the plasma toward the interconnect structure;
  - sputter cleaning the surface oxide from the bottom of the hole with the physical etch component; and

anisotropically removing organic material from displaced from the sidewalls and deposited at the bottom of the hole with the chemical etch component.

11. (Original) The method of claim 10, wherein the chemical etch component comprises nitrogen.
12. (Original) The method of claim 10, wherein the physical etch component comprises argon.
13. (Original) The method of claim 10, wherein the physical etch component comprises helium.
14. (Canceled)
15. (Original) The method of claim 10, wherein the chemical etch is ion enhanced with an RF bias of between about 0 watts and about 500 watts.
16. (Currently Amended) A method of forming an interconnect through an organic ILD; the method comprising:
  - forming a lower conductive layer on a semiconductor substrate;
  - forming the organic ILD on the top surface of said lower conductive layer;
  - etching a hole through the organic ILD down to the lower conductive layer;

performing an RF sputter clean of a surface oxide from the top surface of said lower conductive layer forming the bottom of the hole;

performing an anisotropic, ion enhanced chemical etch of organic ILD material deposited in the hole during said RF sputter clean, wherein the etch is performed at least partially during the RF sputter clean;

forming a plug in the hole; and

forming an upper conductive layer on the organic ILD and the plug.

17. (Original) The method of claim 16, wherein said RF sputter clean comprises using an argon plasma.

18. (Original) The method of claim 16, wherein said RF sputter clean comprises using a helium plasma.

19. (Previously Presented) The method of claim 16, wherein said etch of organic ILD material comprises using a nitrogen plasma.

20. (Canceled)

21. (Previously Presented) The method of claim 26, wherein the anisotropic ion enhanced chemical etch comprises using a nitrogen plasma.

22. (Original) The method of claim 16, further comprising:

forming a lower cap layer on the lower conductive layer before the forming of the organic ILD layer; and

forming an upper cap layer on the organic ILD layer,

wherein the etching of the hole further comprises etching through the upper cap layer and lower cap layer.

23. (Original) The method of claim 16, further comprising forming a liner in the hole before the forming of the plug.

24. (Currently Amended) A method of cleaning a previously etched hole formed in an organic inter-level dielectric (ILD), the hole having a sidewall surface defined by said organic ILD and a bottom comprising a layer of surface oxide on the top surface of a conductive layer, said surface oxide formed during the etching of said hole, the organic ILD disposed on said conductive layer over a semiconductor substrate, the method comprising:

displacing organic ILD particles from said sidewall surface and depositing said displaced organic ILD particles at said bottom of said hole while performing a radio frequency (RF) sputter clean of the ~~hole~~ hole to remove said surface oxide at the bottom of said hole; and

removing organic particles displaced from the sidewalls and deposited at the bottom of the hole during the sputter clean by performing an anisotropic, ion enhanced etch of the hole during at least a portion of the sputter clean.

25. (Canceled)

26. (Previously Presented) A method of forming an interconnect through an organic ILD, the method comprising:

forming a lower conductive layer having a top surface on a semiconductor substrate;

forming the organic ILD on the lower conductive layer;

etching the organic ILD down to the lower conductive layer to define a hole through said ILD comprising a sidewall surface of said organic ILD and a bottom comprising a layer of oxide on the top surface of said lower conductive layer, said layer of oxide formed during said etching step;

displacing particles from said sidewall surface of said organic ILD and depositing said displaced particles at said bottom of said hole while performing an RF sputter clean of the hole to remove said surface oxide on said exposed surface of said lower conductive layer;

performing an anisotropic, ion enhanced chemical etch of organic ILD material in the hole during at least a portion the RF sputter clean to remove said deposited displaced particles;

forming a plug in the hole; and

forming an upper conductive layer on the organic ILD and the plug.

27. (Previously Presented) The method of claim 24 wherein the hole is part of an interconnect structure and wherein a conductive layer is disposed at the bottom of the hole.